# CMOS Integrated DTMF Receiver

## Features

- Full DTMF receiver
- Less than 35mW power consumption
- Industrial temperature range
- Uses quartz crystal or ceramic resonators
- Adjustable acquisition and release times
- 18-pin DIP, 18-pin DIP EIAJ, 18-pin SOIC, 20-pin PLCC
- **CM8870C**
  - — Power down mode
  - — Inhibit mode
  - — Buffered OSC3 output (PLCC package only)
- CM8870C is fully compatible with CM8870 for 18-pin devices by grounding pin 5 and pin 6.

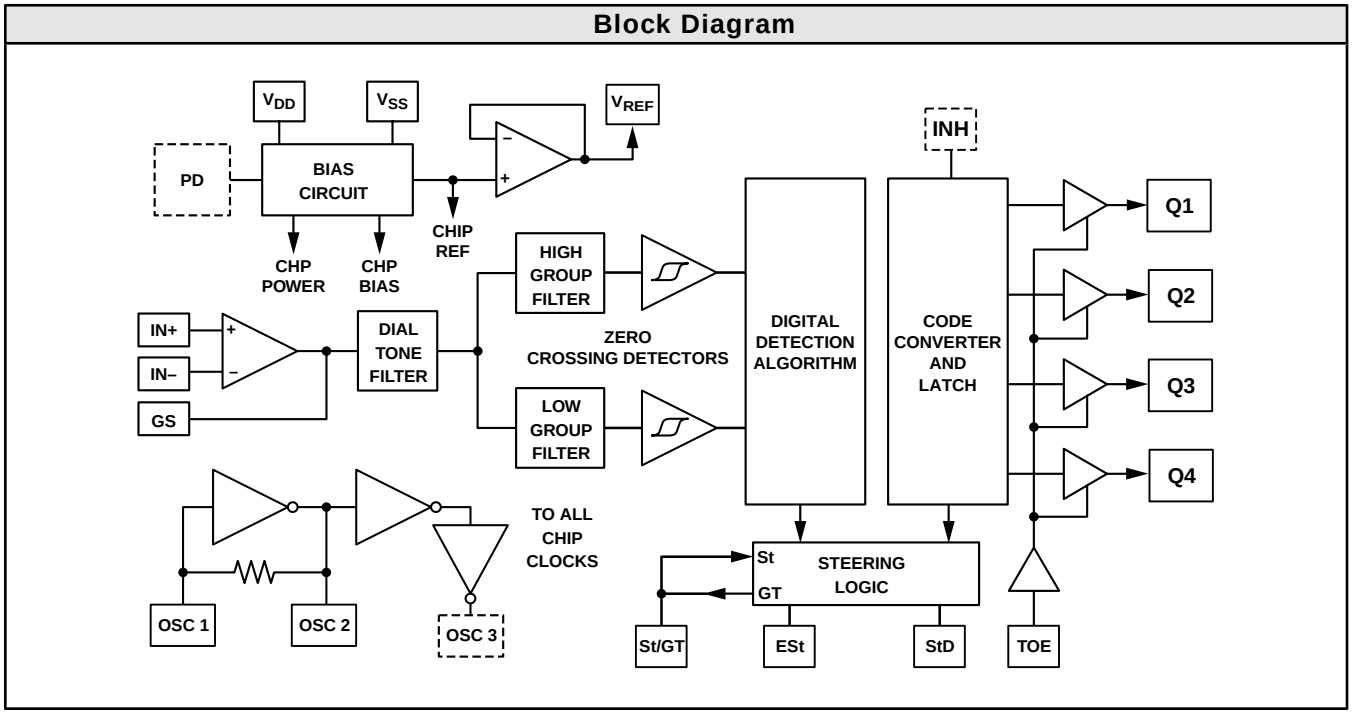
## Applications

- PABX
- Central office
- Mobile radio
- Remote control
- Remote data entry
- Call limiting
- Telephone answering systems
- Paging systems

## Product Description

The CAMD CM8870/70C provides full DTMF receiver capability by integrating both the band-split filter and digital decoder functions into a single 18-pin DIP, SOIC, or 20-pin PLCC package. The CM8870/70C is manufactured using state-of-the-art CMOS process technology for low power consumption (35mW, MAX) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The CM8870/70C decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. This DTMF receiver minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal or ceramic resonator as an external component.

### Block Diagram






C1581000

**Absolute Maximum Ratings:** (Note 1)

| Absolute Maximum Ratings | | |
|---|---|---|
| **Symbol** | **Parameter** | **Value** |
| $V_{DD}$ | Power Supply Voltage ($V_{DD}/V_{SS}$) | 6V MAX |
| Vdc | Voltage on any Pin | $V_{SS}$ – 0.3V to $V_{DD}$ + 0.3V |
| $I_{DD}$ | Current on any Pin | 10mA MAX |
| $T_A$ | Operating Temperature | –40˚C to 85˚C |
| $T_S$ | Storage Temperature | –65˚C to 150˚C |

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

**DC Characteristics:** All voltages referenced to $V_{SS}$, $V_{DD}$ = 5V ±5%, $T_A$ = –40°C to 85°C unless otherwise noted.

| DC Characteristics | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | | **Test Conditions** | **MIN** | **TYP** | **MAX** | **UNIT** |
| $V_{DD}$ | Operating Supply Voltage | | | 4.75 | | 5.25 | V |
| $I_{DD}$ | Operating Supply Current | | | | 3.0 | 7.0 | mA |
| $I_{DDQ}$ | Standby Supply Current | | PD = $V_{DD}$ | | | 25 | µA |
| $P_O$ | Power Consumption | | f = 3.579 MHz; $V_{DD}$ = 5V | | 15 | 35 | mW |
| $V_{IL}$ | Low Level Input Voltage | | $V_{DD}$ = 5V | | | 1.5 | V |
| $V_{IH}$ | High Level Input Voltage | | $V_{DD}$ = 5V | 3.5 | | | V |
| $I_{IH}/L_{IL}$ | Input Leakage Current | | $V_{IN}$ = $V_{SS}$ = $V_{DD}$ (Note 1) | | 0.1 | | µA |
| $I_{SO}$ | Pull Up (Source) Current on TOE | | TOE = 0V, $V_{DD}$ = 5V | | 6.5 | 20 | µA |
| $R_{IN}$ | Input Impedance, (IN+, IN–) | | @ 1KHz | 8 | 10 | | MΩ |
| $V_{Tst}$ | Steering Threshold Voltage | | $V_{DD}$ = 5V | 2.2 | | 2.5 | V |
| $V_{OL}$ | Low Level Output Voltage | | $V_{DD}$ = 5V, No Load | | | 0.03 | V |
| $V_{OH}$ | High Level Output Voltage | | $V_{DD}$ = 5V, No Load | 4.97 | | | V |
| $I_{OL}$ | Output Low (Sink) Current | | $V_{OUT}$ = 0.4V | 1.0 | 2.5 | | mA |
| $I_{OH}$ | Output High (Source) Current | | $V_{OUT}$ = 4.6V | 0.4 | 0.8 | | mA |
| $V_{REF}$ | Output Voltage | $V_{REF}$ | $V_{DD}$ = 5.0V, No Load | 2.4 | | 2.7 | V |
| $R_{OR}$ | Output Resistance | | | | 10 | | kΩ |

**Operating Characteristics:** All voltages referenced to $V_{SS}$, $V_{DD}$ = 5V ±5%, $T_A$ = –40°C to 85°C unless otherwise noted.
**Gain Setting Amplifier**

| Operating Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test Conditions** | **MIN** | **TYP** | **MAX** | **UNIT** |
| $I_{IN}$ | Input Leakage Current | $V_{SS}$ < $V_{IN}$ < $V_{DD}$ | | | ±100 | nA |
| $R_{IN}$ | Input Resistance | | 10 | | | MΩ |
| $V_{OS}$ | Input Offset Voltage | | | | ±25 | mV |
| PSRR | Power Supply Rejection | 1 KHz (Note 12) | 50 | | | dB |
| CMRR | Common Mode Rejection | –3V < $V_{IN}$ < 3V | 40 | | | dB |
| $A_{VOL}$ | DC Open Loop Voltage Gain | | 32 | | | dB |
| fc | Open Loop Unity Gain Bandwidth | | 0.3 | | | MHz |
| $V_O$ | Output Voltage Swing | $R_L \geq 100$ KW to $V_{SS}$ | 4 | | | $V_{P-P}$ |
| $C_L$ | Maximum Capacitive Load (GS) | | | | 100 | pF |
| $R_L$ | Maximum Resistive Load (GS) | | | | 50 | KΩ |
| Vcm | Common Mode Range (No Load) | No Load | 2.5 | | | $V_{P-P}$ |

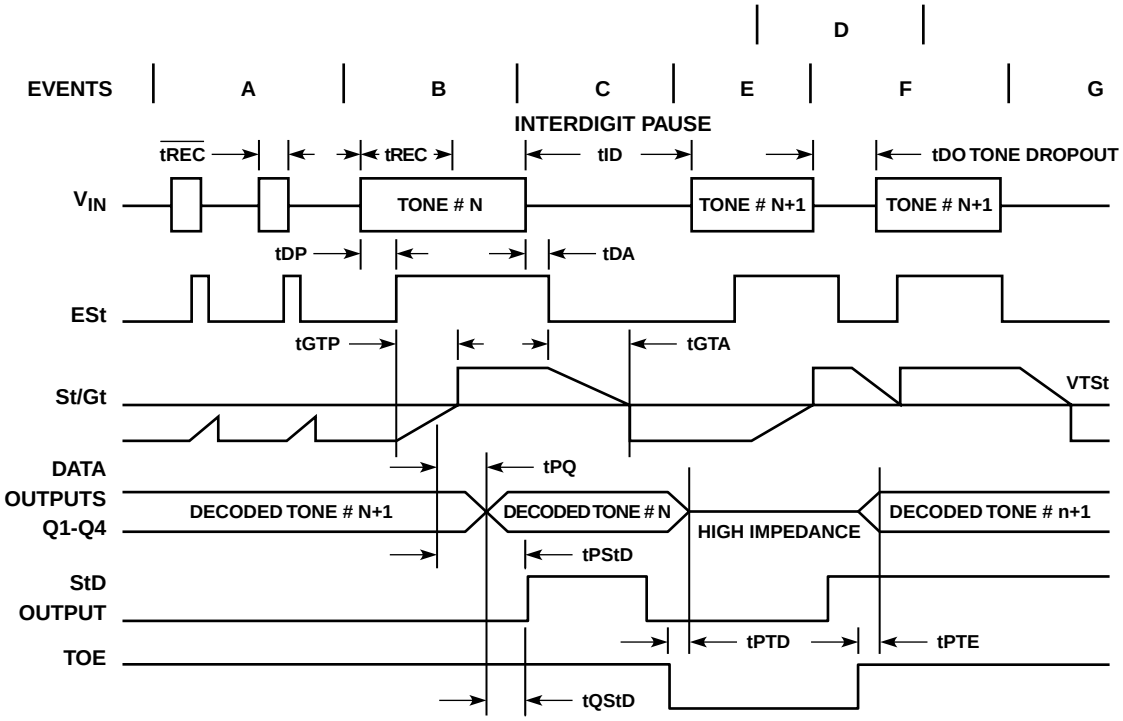
**AC Characteristics:** All voltages referenced to $V_{SS}$, $V_{DD}$ = 5.0V ±5%, $T_A$ = –40°C to +85°C, $f_{CLK}$ = 3.579545 MHz using test circuit in Figure 1 unless otherwise noted.

| AC Characteristics | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | | **Notes** | **MIN** | **TYP** | **MAX** | **UNIT** |
| | Valid Input Signal Levels (each tone of composite signal) | | 1, 2, 3, 4, 5, 8 | –29 | | 1 | dBm |
| | | | | 27.5 | | 869 | $mV_{RMS}$ |
| | Positive Twist Accept | | 2, 3, 4, 8 | | | 10 | dB |
| | Negative Twist Accept | | | | | 10 | dB |
| | Freq. Deviation Aceept Limit | | 2, 3, 5, 8, 10 | | | 1.5%±2Hz | Norm. |
| | Freq. Deviation Reject Limit | | 2, 3, 5 | ±3.5% | | | Norm. |
| | Third Tone Tolerance | | 2, 3, 4, 5, 8, 9, 13, 14 | | –16 | | dB |
| | Noise Tolerance | | 2, 3, 4, 5, 6, 8, 9 | | –12 | | dB |
| | Dial Tone Tolerance | | 2, 3, 4,5, 7, 8, 9 | | 22 | | dB |
| $t_{DP}$ | Tone Present Detection Time | | Refer to Timing Diagram | 5 | 8 | 14 | ms |
| $t_{DA}$ | Tone Absent Dectection Time | | Refer to Timing Diagram | 0.5 | 3 | 8.5 | ms |
| $t_{REC}$ | MIN Tone Duration Accept | | 15 | | | 40 | ms |
| | MAX Tone Duration Reject | | 15 | 20 | | | ms |
| $t_{ID}$ | MIN Interdigit Pause Accept | | 15 | | | 40 | ms |
| $t_{DO}$ | MAX Interdigit Pause Reject | | 15 | 20 | | | µs |
| $t_{PQ}$ | Propagation Delay (St to Q) | | TOE = $V_{DD}$ | | 6 | 11 | µs |
| $t_{PS}t_D$ | Propagation Delay (St to StD) | | TOE = $V_{DD}$ | | 9 | 16 | µs |
| $t_{QS}t_D$ | Output Data Set Up (Q to StD) | | TOE = $V_{DD}$ | | 3.4 | | µs |
| $t_{PTE}$ | Propagation Delay (TOE to Q) | Enable | $R_L$ = 10KΩ | | 50 | | ns |
| $t_{PTD}$ | | Disable | $C_L$ = 50pf | | 300 | | ns |
| $f_{CLK}$ | Crystal/Clock Frequency | | | 3.5759 | 3.5795 | 3.5831 | MHz |
| $C_{LO}$ | Clock Ouput (OSC 2) | Capacitive Load | | | | 30 | pF |

**Notes:**

1. dBm = decibels above or below a reference power of 1mW into a 600Ω load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40ms. Tone pause = 40ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350Hz and 440Hz) ±2%.
8. For an error rate of better than 1 in 10,000
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN–, and TOE.
12. External voltage source used to bias $V_{REF}$.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 1. Input DTMF tone level at –28dBm.
15. Times shown are obtained with circuit in Figure 1 (User adjustable).

## Timing Diagram




## Explanation of Events

A. Tone bursts detected, tone duration invalid, outputs not updated.

B. Tone #n detected, tone duration valid, tone decoded and latched in outputs.

C. End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.

D. Outputs switched to high impedance state.

E. Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).

F. Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.

G. End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

## Explanation of Symbols

| | |
|---|---|
| $V_{IN}$ | DTMF composite input signal. |
| ESt | Early Steering Output. Indicates detection of valid tone frequencies. |
| St/GT | Steering input/guard time output. Drives external RC timing circuit. |
| Q1-Q4 | 4-bit decoded tone output. |
| StD | Delayed Steering Output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal. |
| TOE | Tone Output Enable (input). A low level shifts Q1-Q4 to its high impedance state. |
| $t_{REC}$ | Maximum DTMF signal duration not detected as valid. |
| $t_{REC}$ | Minimum DTMF signal duration required for valid recognition. |
| $t_{ID}$ | Minimum time between valid DTMF signals. |
| $t_{DO}$ | Maximum allowable drop-out during valid DTMF signal. |
| $t_{DP}$ | Time to detect the presence of valid DTMF signals. |
| $t_{DA}$ | Time to detect the absence of valid DTMF signals. |
| $t_{GTP}$ | Guard time, tone present. |
| $t_{GTA}$ | Guard time, tone absent. |

## Functional Description

The CAMD CM8870/70C DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP, SOIC, or 20-pin PLCC package configuration. The CM8870/70C's internal architecture consists of a band-split filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

## Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350Hz and 440Hz which provides excellent dial tone rejection. Each filter output is followed by a single order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

## Decoder Section

The CM8870/70C decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

## Steering Circuit

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by $E_{St}$. A logic high on ESt causes $V_C$ (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (ESt remains high) for the validation period ($t_{GTP}$), $V_C$ reaches the threshold ($V_{TSt}$) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch. At this point, the GT output is activated and drives VC to $V_{DD}$. GT continues to drive high as long as ESt remains high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

## Guard Time Adjustment

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{GTP} = 0.67\ RC$$

The value of $t_{DP}$ is a parameter of the device and $t_{REC}$ is the minimum signal duration to be recognized by the receiver. A value for C of 0.1µF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a $t_{REC}$ of 40ms would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard-times for tone-present ($t_{GTP}$) and tone absent ($t_{GTA}$). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing $t_{REC}$ improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short $t_{REC}$ with a long $t_{DO}$ would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure 5.

## Input Configuration

The input arrangement of the CM8870/70C provides a differential input operational amplifier as well as a bias source ($V_{REF}$) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 1, with the op-amp connected for unity gain and VREF biasing the input at ½ $V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R5.

## Clock Circuit

The internal clock circuit is completed with the addition of a standard television color burst crystal or ceramic resonator having a resonant frequency of 3.579545MHz. The CM8870C in a PLCC package has a buffered oscillator output (OSC3) that can be used to drive clock inputs of other devices such as a microprocessor or other CM887X's as shown in Figure 7. Multiple CM8870/70Cs can be connected as shown in figure 8 such that only one crystal or resonator is required.

**Pin Function**

| Name | Function | Discription |
|---|---|---|
| IN+ | Non-inverting input | Connection to the front-end differential amplifier |
| IN– | Inverting input | Connection to the front-end differential amplifier |
| GS | Gain select | Gives access to output of front-end differential amplifier for connection of feedback resistor. |
| $V_{REF}$ | Reference output Voltage (nominally $V_{DD}$/2) | May be used to bias the inputs at mid-rail. |
| INH | Inhibits detection of tones | Represents keys A, B, C, and D |
| OSC3 | Digital buffered oscillator output | |
| PD | Power down | Logic high powers down the device and inhibits the oscillator. |
| OSC1 | Clock input | 3.579545MHz crystal connected between these pins completes internal oscillator |
| OSC2 | Clock output | 3.579545MHz crystal connected between these pins completes internal oscillator |
| $V_{SS}$ | Negative power supply | Normally connected to OV |
| TOE | Three-state output enable (Input) | Logic high enables the outputs Q1-Q4. Internal pull-up. |
| $Q_1$<br>$Q_2$<br>$Q_3$<br>$Q_4$ | Three-state ouputs | When enabled by TOE, provides the code corresponding to the last valid tone pair received. (See Figure 2). |
| StD | Delayed Steering output | Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low shen the voltage on St/GT falls below $V_{TSt}$. |
| ESt | Early steering output | Presents logic high immediately when the digital algorithm detects a recongnizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low. |
| St/Gt | Steering input/guard time output (bidirectional) | A voltage greater than $V_{TSt}$ detected at St causes the device to register the dectected tone pair. The GT output acts to reset the external steering time constrant, and its state is a function of ESt and the voltage on St. (See Figure 2). |
| $V_{DD}$ | Positve power supply | |
| IC | Internal connection | Must be tied to $V_{SS}$ (for 8870 configuration only). |

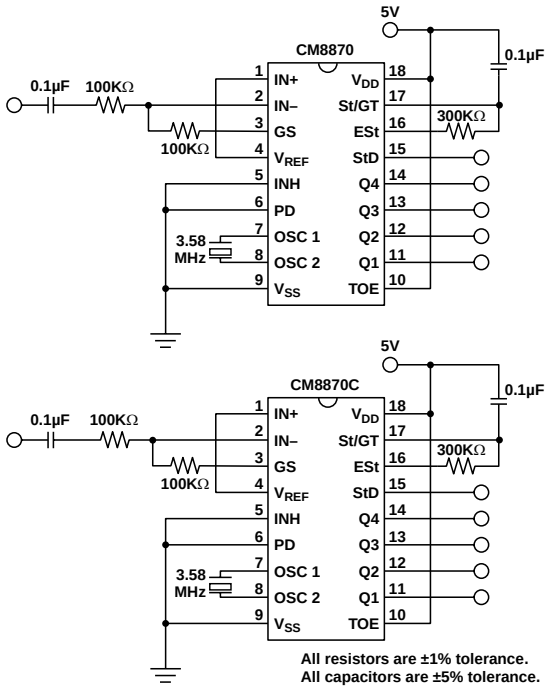



**Figure 1. Single Ended Input Configuration**

| Functional Diode Table | | | | | | | |
|---|---|---|---|---|---|---|---|
| $F_{LOW}$ | $F_{HIGH}$ | KEY | TOW | $Q_4$ | $Q_3$ | $Q_2$ | $Q_1$ |
| 697 | 1209 | 1 | H | 0 | 0 | 0 | 1 |
| 697 | 1336 | 2 | H | 0 | 0 | 1 | 0 |
| 697 | 1477 | 3 | H | 0 | 0 | 1 | 1 |
| 770 | 1209 | 4 | H | 0 | 1 | 0 | 0 |
| 770 | 1336 | 5 | H | 0 | 1 | 0 | 1 |
| 770 | 1477 | 6 | H | 0 | 1 | 1 | 0 |
| 852 | 1209 | 7 | H | 0 | 1 | 1 | 1 |
| 852 | 1336 | 8 | H | 1 | 0 | 0 | 0 |
| 852 | 1477 | 9 | H | 1 | 0 | 0 | 1 |
| 941 | 1336 | 0 | H | 1 | 0 | 1 | 0 |
| 941 | 1209 | * | H | 1 | 0 | 1 | 1 |
| 941 | 1477 | # | H | 1 | 1 | 0 | 0 |
| 697 | 1633 | A | H | 1 | 1 | 0 | 1 |
| 770 | 1633 | B | H | 1 | 1 | 1 | 0 |
| 852 | 1633 | C | H | 1 | 1 | 1 | 1 |
| 941 | 1633 | D | H | 0 | 0 | 0 | 0 |
| - | - | ANY | L | Z | Z | Z | Z |
| L Logic Low, H = Logic, Z = High Impedance | | | | | | | |

**Figure 2. Functional Decode Table**

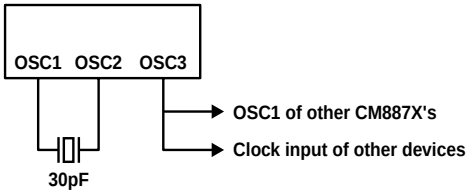



**Figure 7. CM8870C Crystal Connection (PLCC Package Only)**

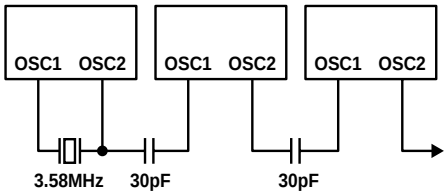
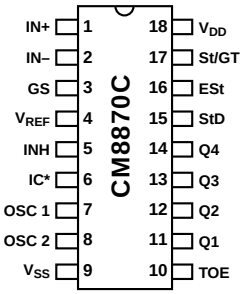
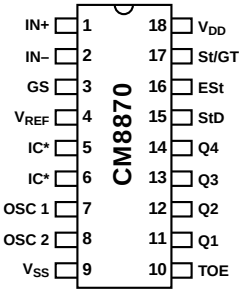



**Figure 8. CM8870/70C Crystal Connection**

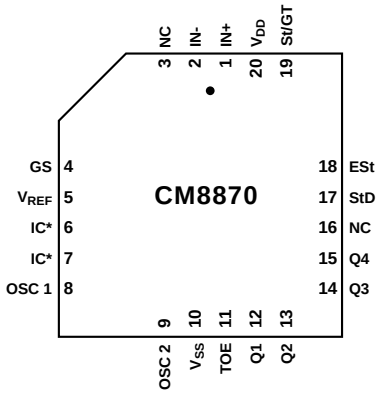
## Pin Assignments



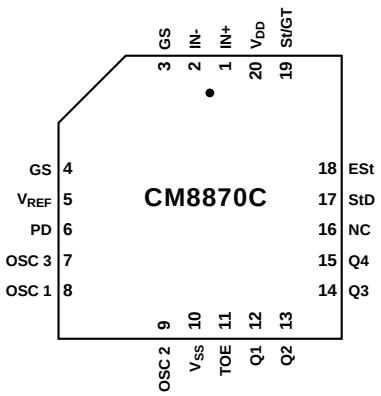

P – Plastic DIP (18)
F – Plastic SOP EIAJ (18)
S – SPIC (18)




P – Plastic DIP (18)
F – Plastic SOP EIAJ (18)
S – SOIC (18)




PE – PLCC (20)
* – Connected to $V_{SS}$




PE – PLCC (20)

## Ordering Information